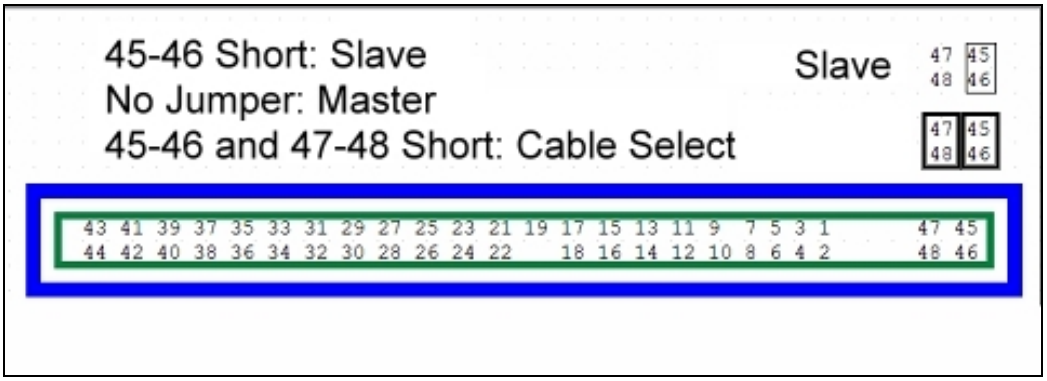
Master/Slave Jumper Select Instruction:



1. **No Jumper: Master (default setting)**
2. **45 - 46 Short: Slave**
3. **45 - 46 and 47 - 48 Short: Cable Select**

Interface Pin Assignment, Signal Names and detail

Description:

DRIVE INTERFACE SIGNALS			
PIN	SIGNAL	PIN	SIGNAL
1	RESET	2	GROUND
3	DD 7	4	DD 8
5	DD 6	6	DD 9
7	DD 5	8	DD 10
9	DD 4	10	DD 11
11	DD 3	12	DD 12
13	DD 2	14	DD 13
15	DD1	16	DD 14
17	DD 0	18	DD 15
19	GROUND	20	KEY
21	DMARQ	22	GROUND
23	DIOW /STOP	24	GROUND
25	DIOR/ -DMARDY HSTROBE	26	GROUND
27	IORDY/-DMARDY/-DSTROBE	28	CSEL
29	DMACK	30	GROUND
31	INTRQ	32	IOCS16
33	DA1	34	PDIAG
35	DA0	36	DA 2
37	CS0	38	CS 1
39	DASP	40	GROUND
41	+5V	42	+5V
43	GROUND	44	RESERVED

Signal List:

SIGNAL NAME	PIN	I/O type	Description
RESET	1	I	This is a reset SIGNAL output from the host system and to be used for interface logic circuit.
DD0-DD15	3-18	I/O	This is a 16-bit bi-directional data bus. The lower 8 bits are used for register access other than data register.
DIOW	23	I	The rising edge of this write strobe signal clocks data from the host data bus into a register on the device.
STOP			Assertion of this signal by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
DIOR	25	I	Activating this read strobe signal enables data from a register on the device to be clocked onto the host data bus. The rising edge of this signal latches data at the host.
HDMARDY			This signal is a flow control signal for Ultra DMA read. Host asserts this signal, and indicates that the host is ready to receive Ultra DMA read data.
HSTROBE			This signal is write data strobe signal from the host for an Ultra DMA write. Both the rising and falling edge latch the data from DD(15:0) into the device.
IORDY	27	O	This signal is used to temporarily stop the host register access (read or write) when the device is Not ready to respond to a data transfer request.
DMARDY			This signal is a flow control signal for Ultra DMA write. Device asserts this signal, and indicates that the device is ready to receive Ultra DMA write data .
DMARDY			This signal is the data in strobe signal from the device for an Ultra DMA read. Both the rising and falling edge latch the data from DD(15:0) into the host.
INTRQ	31	O	This is an interrupt signal for the host system. This signal is asserted by a selected device when the nIEN bit in the Device Control register is "0". In other cases, this signal should be a high impedance state.

Signal List (Continued):

IOCS16	32	I/O	Except for DMA transfers, IOCS16- indicates to the host system that the 16-bit data port has been addressed and that the drive is prepared to send or receive a 16-bit data word. This shall be an open collector output. - When transferring in PIO Mode, if IOCS16- is Not asserted, transfers shall be 8-bit using DD0-7. - When transferring in PIO Mode, if IOCS16- is asserted, transfers shall be 16-bit using DD0-15. - When transferring in DMA Mode, the host shall use a 16-bit DMA channel and IOCS16- shall Not be asserted.
DA0-2	33,35,36	I	This is a register address signal from the host system.
PDIAG	34	I/O	The host shall wait until the power on or hardware reset sequence is complete for all devices on the cable;
CS0-	37	I	This device chip selection signal is used to select the Command Block Registers from the host system.
CS1-	38	I	This device chip selection signal is used to select the Control Block Registers from the host system.
DASP-	39	I/O	This signal indicates that a device is active when the power is turned on. Upon receipt of a command from the host, the device asserts this signal. At command completion, the device de-asserts this signal.
DMARQ	21	O	The device shall assert this signal, used for DMA data transfers between host and device, when it is ready to transfer data.
DMACK	29	I	The host in response to DMARQ to either acknowledge that data has been accepted, or that data is available shall use this signal.
CSEL	28	I	The device is configured as either Device 0 (Master) or Device 1 (Slave) depending upon the signal level of 28 pin CSEL signal. - When used as Device 0 (Master), CSEL is open - When used as Device 1 (Slave), the host shall have pull-up resistor. Recommended pull-up resistor is 10K ohm.
Ground	2, 19, 22,24, 26, 30, 40, 43	P	Ground Pin
Power	41, 42	P	5v power Pin

DIMENSION: