2011

Renice X2 1.8” micro SATA SSD DATA Sheet

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CATALOGUE

1. Introduction

1.1 Product Overview

Renice 1.8 inch MicroSATA SSD (Solid State Drive) is a high performance and high reliability storage device based on NAND Flash technology that designed to solve the bottleneck of computing system by traditional hard disk drives. With no moving parts and sharing the same host interface and same physical dimension with Hard Disk Drive, Renice 1.8 inch MicroSATA SSD can be drop-in replaced with the hard disk drives without anything. With a high performance and low power consumption, it can be a good storage device for NB and Tablet PC, it purely consists of semiconductor devices and NAND flash memories, which give rugged features against shock and vibration using in extreme environment such as industrial PC an increased MTBF. Further more, Renice 1.8 inch MicroSATA SSD has highly advanced flash memory management algorithm to guarantee higher performance and data integrity.

1.2 Feature

● Performance
Sequential Data Read/Write:
240/160MB/s (MLC)
250/200MB/s (SLC)
● Form factor: 1.8-inch (78.5.0mm x 54.0mm x 5.0mm) L×W×H
● Interface standard: SATAII revision 2.6
● Density: 8GB, 16GB, 32GB, 64GB, 128GB
● Input voltage: 3.3V (±5%)
Industrial operating temperature range form -40 to +85℃
● Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm
● Supports dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology)
● H/W ECC and EDC for NAND Flash
6,12bytes/sector correctable by RS mode
8,12,16bits/sector correctable by BCH mode
● Write endurance: >8 years @ 100GB write/ day(32GB)
● Read endurance: unlimited
● Data retention: 10 years
● MTBF:2,000,000 Hours

2. Functional Block Diagram

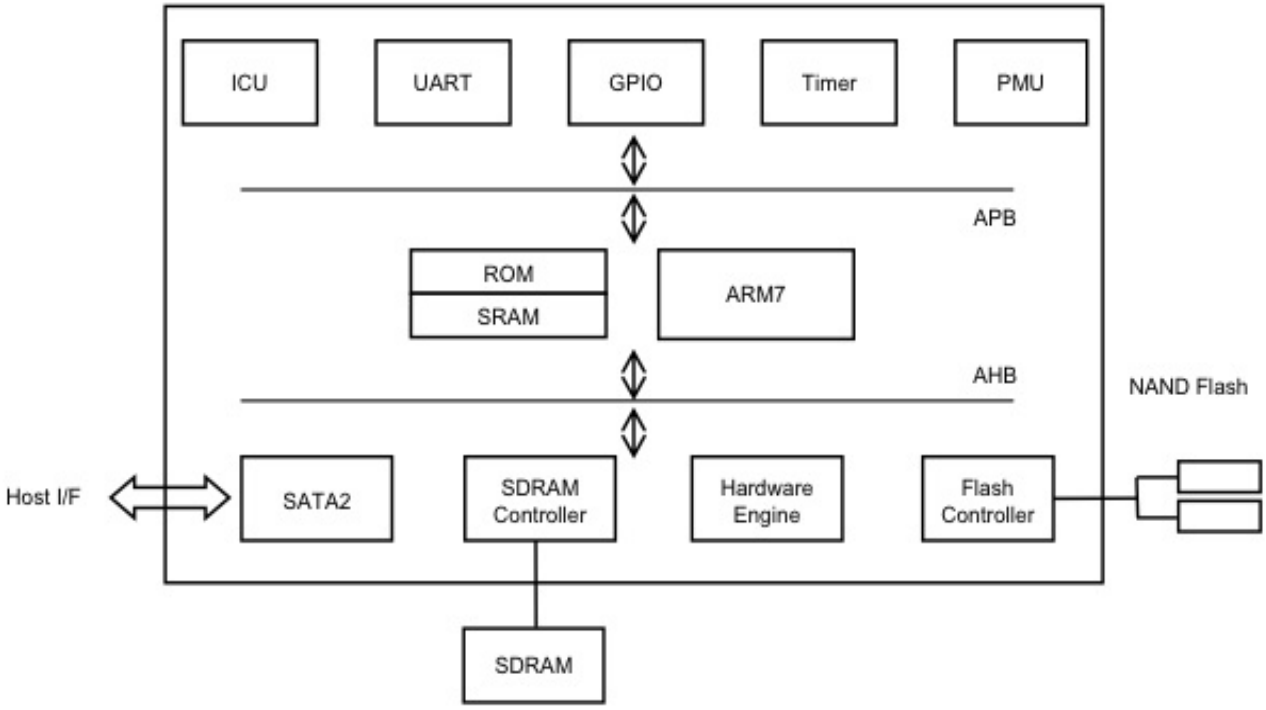
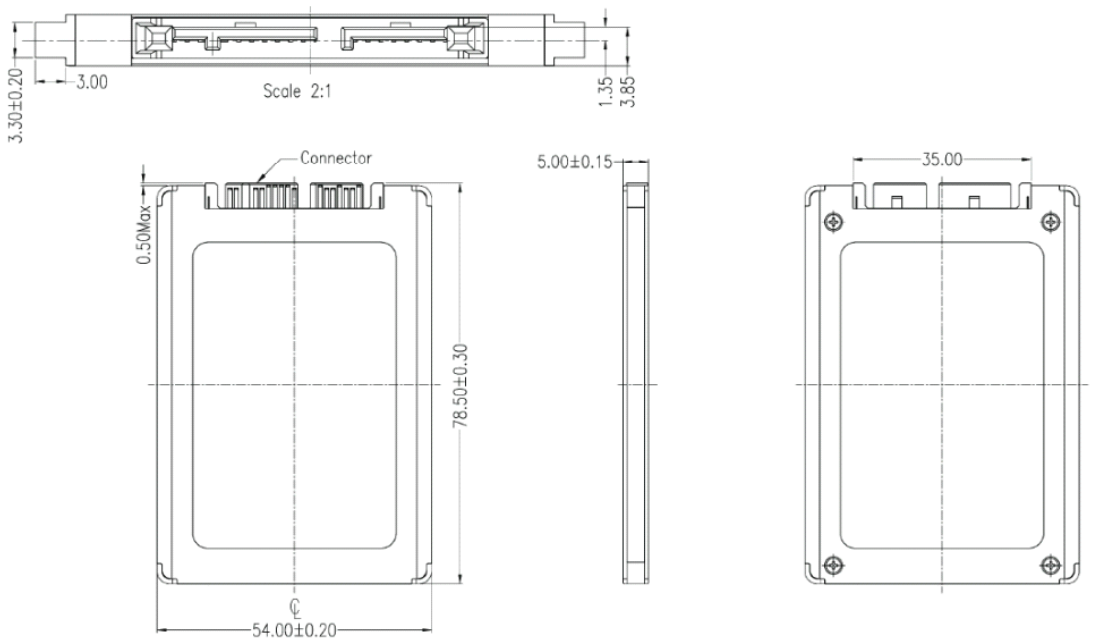


Figure 1: Block Diagram

3.Product Specifications

3.1 Physical Specifications

Form Factor		**1.8 INCH**
Dimensions	**Length**	**78.5mm**
	Width	**54.0mm**
	Height	**5.0mm**
Weight		**<20g**
Connector		**MicroSATA (uSATA) 7+7+2 pin**



3.2 Host Interface

Fully compliant with SATA revision 2.6, compatible with SATA 1.5Gb/s and 3.0Gb/s interface rates
Fully compliant with ATA-7 Standard
PIO, DMA, UDMA(up to 6, dependant on host) supported
SATA 3.0Gb/s Native Command Queuing (NCQ): up to 32 commands
Asynchronous Signal Recovery
Device Activity Signal

3.3 Internal MROM for Boot-loader

Robust Firmware Corruption
Maintenance and diagnostics program in MROM for recovering from drive malfunction

3.4 H/W Acceleration Engine

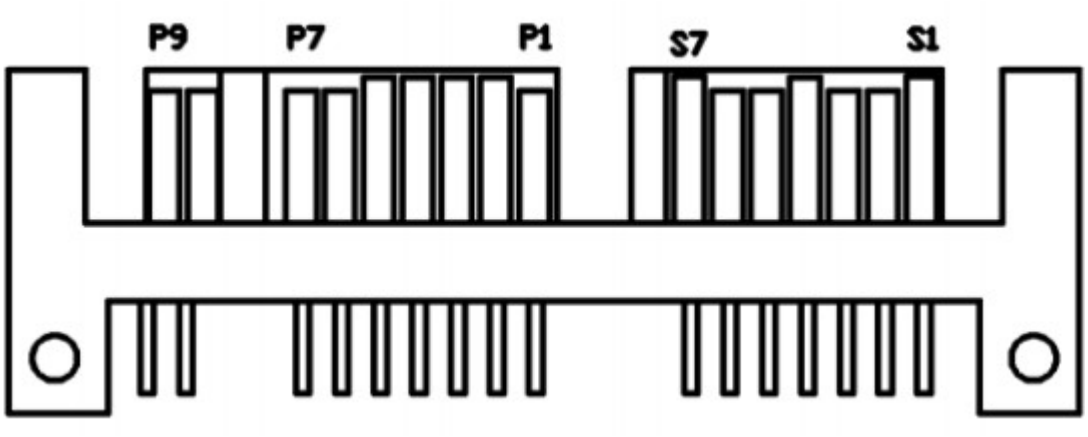
Internal SRAM and external DRAM search engine

3.5 Mobile SDRAM Interface

16MB ~ 64MB buffer memory by Flash capacity

4. Interface Description

4.1 Pin Assignment



4.2 Pin Description

Pin#	SignalName	Description
S1	GND	2nd mate
S2	A+	Differential signalpair A From physicallayer electronics
S3	A-	
S4	GND	2nd mate
S5	B-	Differential signalpair B From physicallayer electronics
S6	B+	
S7	GND	2nd mate
P1	V33	3.3VPower
P2	V33	3.3VPower
P3	GND	1st mate
P4	GND	2nd mate
P5	V5	5VPower,pre-charge, 2nd mate(UN)
P6	V5	5V Power(UN)
P7	NC	
P8	NC	
P9	NC	

5. Electric Specifications

5.1 Power Specification

Operating voltage: 3.3V (±5%)

5.2 Power Supply Voltage

1.0V for Core, 3.3V for NAND, 1.8V for SDRAM

5.3 Power Consumption (typical)

Operation (Read/Write) – 1.42W
Idle – 0.33W
Sleep (Partial/Slumber) – 0.33W/0.1W

6. Reliability Specification

6.1 Environment

Item	Features	
Temperature	Operating	Standard：0~70℃
		Industrial：-40~85℃
Humidity	5-95%	
Vibration	20G(7-2000HZ)	
Shock	2,000G(@0.3ms half sine wave)	

6.2 Wear-leveling

Renice SSD support both static and dynamic wear-leveling, These two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage

6.3 Endurance

Write endurance: >8 years @ 100GB write/ day(32GB)
Read endurance: unlimited

6.4 H/W ECC and EDC for NAND Flash

6,12bytes/sector correctable by RS mode
8,12,16bits/sector correctable by BCH mode

6.5 MTBF

MTBF(Mean Time between Failures) of Renice SSD：2,000,000 hours
Data retention
Data retention at 25℃ of Renice SSD:>10 years

7. Supported ATA Command Lists

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
CHECK POWER MODE	E5h or 98h	SET FEATURES	-
DEVICE CONFIGURATION	-	Enable write cache	EFh/02h
DEVICE CONFIGURATION FREEZE LOCK	B1h/C1h	Set transfer mode	EFh/03h
DEVICE CONFIGURATION IDENTIFY	B1h/C2h	Enable Device-initiated interface power state transitions	EFh/10h/03h
DEVICE CONFIGURATION RESTORE	B1h/C0h	Disable Device-initiated interface power state transitions	EFh/10h/03h
DEVICE CONFIGURATION SET	B1h/C3h	SET MAX	-
DOWNLOAD MICROCODE	92h	SET MAX ADDRESS	F9h/na
EXECUTE DEVICE DIAGNOSTIC	90h	SET MAX FREEZE LOCK	F9h/04h
FLUSH CACHE	E7h	SET MAX LOCK	F9h/02h
FLUSH CACHE EXT	EAh	SET MAX SET PASSWORD	F9h/01h
IDENTIFY DEVICE	ECh	SET MAX UNLOCK	F9h/03h
IDLE	E3h or 97h	SET MAX ADDRESS EXT	37h
IDLE IMMEDIATE	E1h or 95h	SET MULTIPLE MODE	C6h
INITIALIZE DEVICE PARAMETERS	91h	SLEEP	E6h or 99h
NOP	00h/00h	SMART	-
READ BUFFER	E4h	SMART DISABLE OPERATIONS	B0h/D9h
READ DMA	C8h	SMART ENABLE OPERATIONS	B0h/D8h
READ DMA EXT	25h	SMART EXECUTE OFF-LINE IMMIDIATE	B0h/D4h
READ FPDMA QUEUED	60h	SMART READ DATA	B0h/D0h
READ LOG EXT	2Fh	SMART READ LOG	B0h/D5h
READ MULTIPLE	C4h	SMART RETURN STATUS	B0h/DAh
READ MULTIPLE EXT	29h	SMART SAVE ATTRIBUTE VALUES	B0h/D3h
READ NATIVE MAX ADDRESS	F8h	SMART WRITE LOG	B0h/D6h
READ NATIVE MAX ADDRESS EXT	27h	STANDBY	E2h or 96h
READ SECTOR(S)	20h	STANDBY IMMEDIATE	E0h or 94h
READ SECTOR(S) EXT	24h	WRITE BUFFER	E8h
READ VERIFY SECTOR(S)	40h	WRITE DMA	CAh
READ VERIFY SECTOR(S) EXT	42h	WRITE DMA EXT	35h
SECURITY DISABLE PASSWORD	F6h	WRITE FPDMA QUEUED	61h
SECURITY ERASE PREPARE	F3h	WRITE LOG EXT	3Fh
SECURITY ERASE UNIT	F4h	WRITE MULTIPLE	C5h
SECURITY FREEZE LOCK	F5h	WRITE MULTIPLE EXT	39h
SECURITY SET PASSWORD	F1h	WRITE SECTOR(S)	30h
SECURITY UNLOCK	F2h	WRITE SECTOR(S) EXT	34h
SEEK	70h		

8. SMART

8.1 SMART subcommand sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Command	Command Code (Hex)
SMART READ DATA	D0h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
SMART READ LOG	D5h
SMART WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh

8.2 SMART Read Data (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. The Attribute Values consist of 512bytes.

8.2.1 Device Attribute Data Structure

Byte	Description
0~1	Data structure revision number (Vendor Specific)
2~361	1st - 30th Individual attribute data (Vendor Specific)
362	Off-line data collection status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point (Vendor Specific)
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374-510	Reserved
511	Data structure checksum

8.2.2 Individual Attribute Data Structure

Byte	Description
0	Attribute ID Number
1~2	Status Flag
3~10	Attribute Value (FFFF FFFF FFFF FFFFh)
11	Reserved

8.2.3 Attribute ID Numbers

ID	Attribute Name	ID	Attribute Name
1[1)]	Raw Read Error Rate	202	Total Count of Error Bits from Flash
9	Power-On Hours	203	Total Count of Read Sectors with Correctable Errors
12	Power Cycle Count	204	Bad Block Full Flag
184	Initial Bad Block Count	205	Maximum PE Count Specification
195	Program Failure Block Count	206	Minimum Erase Count
196	Erase Failure Block Count	207	Maximum Erase Count
197	Read Failure Block Count (Uncorrectable)	208	Average Erase Count
198	Total Count of Read Sectors	209[2)]	Remaining Life(%)
199	Total Count of Write Sectors	211	SATA Error Count CRC
200	Total Count of Read Commands	212	SATA Error Count Handshake
201	Total Count of Write Commands		

1) indicates that the corresponding Attribute Values is fixed value for compatibility.

2) Remaining Life [%] = MIN(Remaining Life by Erase Count, Remaining Life by Bad Block)

-. Remaining Life by Erase Count = 100 – (average erase count / Max_PE_Count)

-. Remaining Life by Bad Block = 100 – (runtime bad block number of Bad Bank / Bad_BLK_Max of Bad Bank)

-. Max_PE_Count is defined by NAND Flash specification

-. Bad_BLK_Max is the number defined by firmware excluding the initial bad blocks.

-. Bad Bank is the bank which has the biggest number of bad blocks among banks.

8.3 SMART Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature.

8.4 SMART Execute Off-line Immediately (subcommand D4h)

This subcommand causes the device to start the off-line process for the requested mode and operation. The LBA Low register shall be set to specify the operation to be executed.

LBA Low	Description
00h	Execute SMART off-line data collection routine immediately
01h	Execute SMART Short self-test routine immediately in off-line mode
02h	Execute SMART Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute SMART Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute SMART short self-test routine immediately in captive mode
82h	Execute SMART Extended self-test routine immediately in captive mode
84h	Execute SMART selective self-test routine immediately in captive mode
C0h	Reserved

8.5 SMART Read Log Sector (subcommand D5h)

This command returns the specified log sector content to the host.
LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

Log Sector Address	No. Sector	Content	
00h	1	Log directory	Read Only
01h	1	SMART error log	Read Only
02h	1	Comprehensive SMART error log	Read Only
04h-05h	-	Reserved	Read Only
06h	1	SMART self-test log	Read Only
08h	-	Reserved	Read Only
09h	1	Selective self-test log	Read and Write
0Ah-7Fh	-	Reserved	Read Only
80h-9Fh	16	Host vendor specific	Read and Write
A0h-FFh	-	Reserved	Vendor Specific

8.5.1 SMART Log Directory

Byte	Description
0~1	SMART Logging Version (set to 01h)
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
...	
510	Number of sectors in the log at log address 255
511	Reserved

8.5.2 SMART summary error log sector

Byte	Description
0	SMART error log version (set to 01h)
1	Error log index
2~91	First error log data structure
92~181	Second error log data structure
182~271	Third error log data structure
272~361	Fourth error log data structure
362~451	Fifth error log data structure
452~453	Device error count
454~510	Reserved
511	Data Structure checksum

Error log data structure

Byte	Description
n ~ n+11	First command data structure
n+12 ~ n+23	Second command data structure
n+24 ~ n+35	Third command data structure
n+36 ~ n+47	Fourth command data structure
n+48 ~ n+59	Fifth command data structure
n+60 ~ n+89	Error data structure

Command data structure

Byte	Description
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Error data structure

Byte	Description
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 – n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
3h	xActive/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique

8.5.3 Self-test log structure

Byte	Description
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
.....	.....
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

N is 0 through 20.

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors have been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor.

When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

8.5.4 Selective self-test log structure

Byte	Content	
0-1	Data structure revision	Read and Write
2-9	Starting LBA for test span 1	Read and Write
10-17	Ending LBA for test span 1	Read and Write
18-25	Starting LBA for test span 2	Read and Write
26-33	Ending LBA for test span 2	Read and Write
34-41	Starting LBA for test span 3	Read and Write
42-49	Ending LBA for test span 3	Read and Write
50-57	Starting LBA for test span 4	Read and Write
58-65	Ending LBA for test span 4+	Read and Write
66-73	Starting LBA for test span 5	Read and Write
74-81	Ending LBA for test span 5	Read and Write
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags R/W	Read and Write
504-507	Vendor Specific	Vendor specific
508-509	Selective self test pending time	Read and Write
510	Reserved	Reserved
511	Data structure checksum	Read and Write

8.6 SMART Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. LBA Low and Sector Count registers shall be set to specify the log address and sector number to be written.

8.7 SMART Enable Operations (subcommand D8h)

This subcommand enables access to all SMART capabilities. Prior to receipt of a SMART Enable

Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

8.8 SMART Disable Operations (subcommand D9h)

This subcommand disables all SMART capabilities. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.
After receipt of the SMART Disable Operations subcommand from the host, all other SMART subcommands except SMART Enable Operations are disabled and will be aborted by the device returning the error code as specified in —SMART Error Codes ‖ .
Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or a SMART Save Attribute Values command.

8.9 SMART Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

8.10 SMART Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities. The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count Feature Description

00h Disable Automatic Off-line
F8h Enable Automatic Off-line
A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some

other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence. A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in ―SMART Error Codes‖.

9. Security

9.1 Default setting

The Flash SSD is shipped with master password set to 20h value (ASCII blanks) and the lock function disabled. The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

9.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on.

9.3 SECURITY mode operation from power-on

In locked mode, the Flash SSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

9.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data. However, the drive can be unlocked using the master password.
If the user password is lost and Maximum security level is set, it is impossible to access data. However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

10. SATA Optional Features

10.1 Power Segment Pin P11

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications.

10.2 Asynchronous Signal Recovery

Phy may support asynchronous signal recovery for those applications where the usage model of device insertion into a receptacle(power applied at time of insertion) does not apply.
When signal is lost, both the host and the device may attempt to recover the signal. A host or device shall determine loss of signal as represented by a transition from PHYRDY to PHYRDYn, which is associated with entry into states LSI: NoCommErr or LS2:NoComm within the Link layer. Note that negation of PHYRDY does not always constitute a loss of signal. Recovery of the signal is associated with exit from state LS2:NoComm.
If the device attempts to recover the signal before the host by issuing a COMINIT, the device shall return its signature following completion of the OOB sequence which included COMINIT. If a host supports synchronous signal recovery, when the host receives an unsolicited COMINIT, the host shall issue a COMRESET to the device. An unsolicited COMINIT is a COMINIT that was not in response to a preceding COMRESET, as defined by the host not being in the HP2:HR_AwaitCOMINIT state when the COMINIT signal is first received.
When a COMRESET is sent to the device in response to an unsolicited COMINIT, the host shall set the Status register to 7Fh and shall set all other Shadow Command Block Registers to FFh. When the COMINIT is received in response to the COMRESET which is associated with entry into state HP2B:HR_AwaitNoCOMINIT, the Shadow Status register value shall be updated to either FFh or 80h to reflect that a device is attached.

10.3 Native Command Queuing

The device supports the Native Command Queuing (NCQ) command set, which includes READ FPDMA QUEUED and WRITE FPDMA QUEUED commands with a maximum queue depth equal to 31.

11. Identify Device Parameters

Word	Contents	Description
0	0C5Ah	General information
1	3FFFh	Number of logical cylinders
2	C837h	Specific configuration
3	0010h	Number of logical heads
4 – 5	0	Retired
6	003Fh	Number of logical sectors per logical track
7 – 8	0	Reserved
9	0000h	Retired
10 -19	XXXX	Serial number(20 ASCII characters)
20	0000h	Retired
21	4000h	Buffer Memory Size
22	3000h	Obsolete
23 - 26	XXXX	Firmware revision (8 ASCII characters)
27- 46	XXXX	Model number
47	8010h	Number of sectors on multiple commands
48	0000h	Reserved
49	2F00h	Capabilities
50	4000h	Capabilities
51 - 52	0200h	PIO Mode support
53	0007h	Reserved
54	3FFFh	Number of current logical cylinders
55	0010h	Number of current logical heads
56	003Fh	Number of current logical sectors per track
57	FC10h	Obsolete
58	00FBh	
59	0110h	Multiple sector setting
60	XXXXh	Total number of user addressable sectors (LBA mode only)
61	XXXXh	
62	0000h	Obsolete
63	0007h	Multi-word DMA transfer
64	0003h	Flow control PIO transfer modes supported
65	0078h	Minimum Multiword DMA transfer cycle time per word
66	0078h	Manufacturer's recommended Multiword DMA transfer cycle time per word
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with IORDY flow control
69 - 74	0	Reserved
75	001Fh	Queue Depth
76	0706h	Serial ATA capability
77	0000h	Reserved
78	004Ch	Serial ATA features supported
79	0048h	Serial ATA features enabled
80	00E0h	Major Version Number
81	0000h	Minor Version Number
82	346Bh	Command sets supported
83	7D21h	Command sets supported
84	4022h	Command set/feature supported extension
85	3469h	Command set/feature enabled
86	3C01h	Command set/feature enabled
87	4022h	Command set/feature default
88	407Fh	Ultra DMA transfer
89	0000h	Time required for security erase unit completion
90	0000h	Time required for Enhanced security erase completion
91	0000h	Current advanced power management value
92	0000h	Master Password Revision Code
93	0000h	COMRESET result
94	0000h	Automatic acoustic management value
95	0000h	Stream minimum request size
96 - 99	0	Reserved
100 - 103	XXXX	Maximum user LBA for 48bit address feature set
104-105	0	Reserved
106	0000h	Physical sector size / logical sector size
107	0000h	Reserved
108 - 111	XXXX	Unique ID
112 - 116	0	Reserved
117 - 118	0	Words per logical sector
119 - 126	0	Reserved
127	0000h	Removable media status notification feature set supported
128	XXXXh	Security status
129 - 159	0	Undefined
160-254	0	Reserved
255	XXXXh	Integrity word

12. Buy Information

Capacity		
	MLC	SLC
8GB	RIM008-SX21	RIS008-SX21
16GB	RIM016-SX21	RIS016-SX21
32GB	RIM032-SX21	RIS032-SX21
64GB	RIM064-SX21	RIS064-SX21
128GB	RIM128-SX21	RIS128-SX21
256GB	RIM256-SX21	N/A
512GB	RIM512-SX21	N/A

13. Product Part Number Naming Rule