2014

RENICE X9 2.5” SATA III SSD Data Sheet

Renice Technology Co., Limited

2014-1-15

CATALOGUE

1. Introduction

1.1 Product Overview

Renice X9 is an advanced SATA III storage device with superior performance and reliability. Based on a newest SSD controller technology, X9 delivers excellent 4K Random transfer speed, low power consumption and advanced flash memory management algorithm. Targeted at high end applications, X9 is designed with power failure protection, along with over voltage and inrush current protection, making X9 a stable storage device for industrial and military use. Meanwhile, data encryption and Secure Erase are optional for those clients who pay close attention to data security.

1.2 Feature

● **Interface standard:** Serial ATA III 6.0Gbps (Backward compatible with SATA 1.5&3.0Gbps)
● **Performance:**
- Sequent Data Read: up to 530MB/s
- Sequent Data Write: up to 500MB/s
- 4kb Random Read IOPS: up to 70,000
- 4kb Random Write IOPS: up to 65,000
- Access Time: less than 0.1ms
● **Form factor:** 2.5 inch 100.0mm X 70.0mm X 9.0mm (L x W x H)
● **Capacities:**
- MLC: 8GB, 16GB, 32GB, 64GB, 128GB, 256GB 512GB 640GB
- SLC: 8GB, 16GB, 32GB, 64GB, 128GB, 256GB 512GB 640GB
● **Input voltage:** 5.0V (±5%)
● **Temperature ranges:**
- Operation Temp.: 0 ~ +70℃ (Standard) -40 ~ +85℃ (Industrial)
- Storage Temp.: -55 to +95℃
● **Intelligent features:**
- Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm
- Less physical stress to the NAND Flash cell by enhanced data scramble algorithm
- Defect management to extend NAND Flash life cycle
- Supports dynamic power management and S.M.A.R.T
- H/W ECC and EDC: 4~64 bits/ 1Kbytes correctable by BCH-ECC
- Performance Optimization: TRIM (requires OS support)
- Full disk encryption with AES 128/256: ECB/ CBC/ CTR mode support (Optional)
- Power Lost protect and Sudden power-off recovery function support

- Over voltage and inrush current protection support
- Secure Erase function support
- Write endurance: >8 years @ 100GB write/ day (32GB SLC SSD)
- Read endurance: unlimited
- Data retention: JESD47 compliant
- MTBF: >4,000,000 Hours

2. Functional Block Diagram

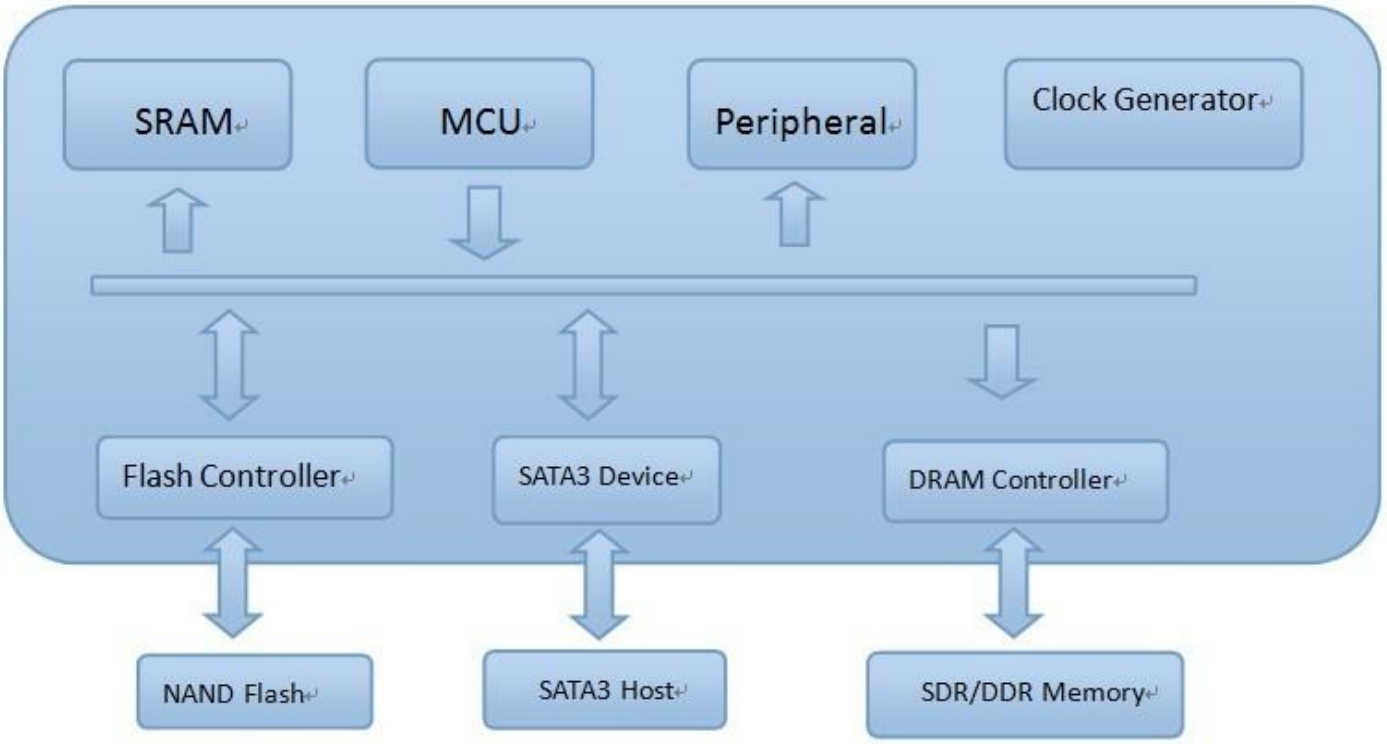

Figure 1: Functional Block Diagram

2.1 Internal ROM for Boot-loader

Robust Firmware Corruption: Maintenance and diagnostics program in MROM for recovering from drive malfunction

2.2 H/W memory Accelerate

Internal SRAM and external DRAM search engine to dramatically increase random performance

2.3 Mobile SDRAM interface

1.8V power supply and LVCMOS compatible

Support Mobile functions: PASR, DPD, Internal TCSR and Programmable Drive Strength

2.4 NAND Flash interface

Independent 10-channels and 8-way interleaving with x8 bus in each channel

Built-in ECC function (BCH-ECC) 4~64 bit correction per 512/1024bytes

On-The-Fly EDC and ECC parity bytes encode

NAND Flash Channel and Bank Architecture

3. Product Specifications

3.1 Physical Specifications

Form factor		2.5 inch
Dimensions(mm)	Length	100.0±0.25 mm
	Width	70.0±0.25 mm
	Height	9.0±0.25 mm
Weight		<76g
Connector		7+15PIN SATAIII 6Gbps

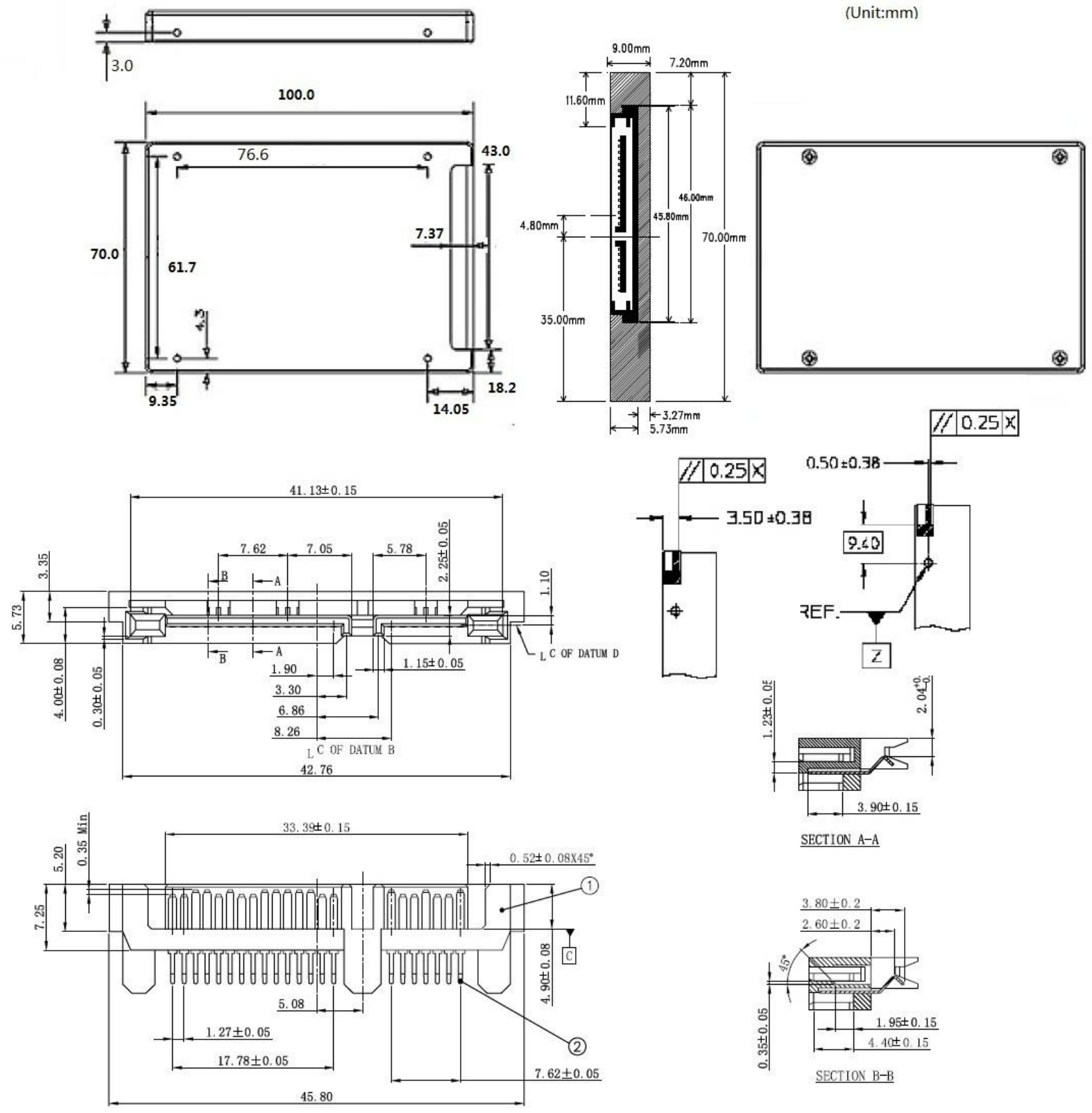

Figure 2: Form factor dimension

3.2 Host Interface

- SATA I, II, III (6Gbps)
- SATA BIST over host and device links
- PIO 0~4 mode
- Up to UDMA mode6 (Ultra DMA133)
- Fully compatible with SATA revision 3.0 Gold
- Fully compliant with ATA-8 Standard including ATA8-ACS2
- SATA 3.0 Native Command Queuing (NCQ): up to 32 commands
- Asynchronous Signal Recovery
- Power Saving Modes: HIPM and DIPM (Partial/Slumber mode)
- Device Activity Signal / Staggered Spin-up
- SATA Cache Module

4. Interface Description

4.1 Pin Assignment

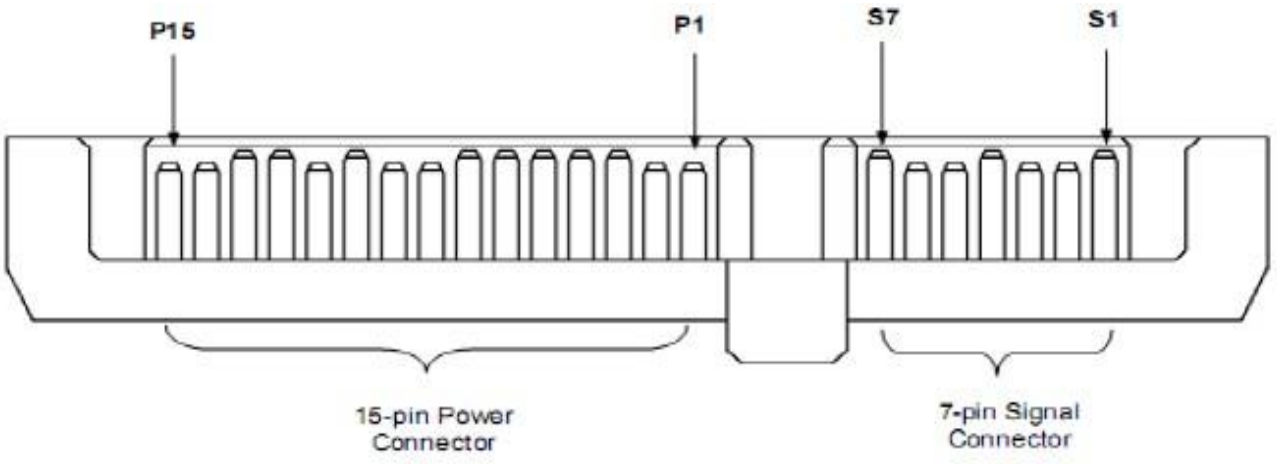

Figure 3: Pin Assignment

4.2 Pin Description

Table .2-2:Connector Pin Signal Definitions

Pin	Definitions
S1	GND
S2	SATA Differential RX+ based on SSD
S3	SATA Differential RX- based on SSD
S4	GND
S5	SATA Differential TX- based on SSD
S6	SATA Differential TX+ based on SSD
S7	GND
P1	+3.3V(Unused)
P2	+3.3V(Unused)
P3	+3.3V(Unused)
P4	GND

Pin	Definitions
P5	GND
P6	GND
P7	+5V
P8	+5V
P9	+5V
P10	GND
P11	DAS/DSS
P12	GND
P13	+12V(Unused)
P14	+12V(Unused)
P15	+12V(Unused)

5. Power Specifications

5.1 Power Specification

- Operating voltage: 5.0V (±5%)
- Power Supply Voltage: 1.2V (for Core)/1.8V(for DDR IO,NAND IO)/3.3V(for Core, NAND IO, GPIO)

Symbol	Min	Typ	Max	Unit	Item
VDDI_33	3.0	3.3	3.6	v	1.8~3.3V Digital Power for I/O
	1.7	1.8	1.9	v	1.8~3.3V Digital Power for I/O
VDDC	1.08	1.2	1.32	v	1.2V Digital Power for Core
VDDI_18	1.7	1.8	1.9	v	1.8V Digital Power for DRAM Interface
vdda	1.08	1.2	1.32	v	1.2V Analog Power for SATA PHY
vddha	1.08	3.3	3.6	v	3.3V Analog Power for SATA PHY
SERVDDDIG1	1.08	1.2	1.32	v	1.2V Digital Power for SATA PHY
SERVDDDIG2	1.08	1.2	1.32	v	1.2V Digital Power for SATA PHY
AVDD_PLL	1.08	1.2	1.32	v	1.2V Analog Power for PLL Core
DVDD_PL	1.08	1.2	1.32	v	1.2V Digital Power for PLL Core
VDDPOC_PLL	3.0	3.3	3.6	v	3.3V Digital Power for PLL I/O pad
VDD_PLL	1.08	1.2	1.32	v	1.2V Digital Power for PLL I/O pad

5.2 Power Consumption (typical)

Parameter	Min	Typ	Max	Unit	Items
Pd operating	-	0.45	-	W	Power Dissipation in idle mode
Pd operating	-	0.6	-	W	Power Dissipation in operating mode
Pd operating	-	0.58	-	W	Power Dissipation in partial mode
Pd operating	-	0.45	-	W	Power Dissipation in slumber mode

* Without DDR IO, NAND IO power consume

6. Reliability Specification

Item	Features	
Temperature	Operation	Standard: 0~70°C
		Industrial: -40~+85°C
	Storage	-55~+95°C
Humidity	0°C to 55°C / 90~98% RH	
Vibration	10Hz-2000Hz, 16.4 G (X, Y, Z axis, 1 hour /axis)	
Shock	Peak Acceleration: 1,500 G, 0.5ms(Half-sine wave, ±X,±Y,±Z axis, 1 time/axis) Peak Acceleration: 50 G, 11ms(Half-sine wave, ±X,±Y,±Z axis, 3 times/axis)	

6.1 Wear-leveling

Renice X9 2.5” SATAIII SSD supports both static and dynamic wear-leveling; these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

6.2 Endurance

Write endurance: >8 years @ 100GB write/ day (32GB SLC SSD)
Read endurance: unlimited

6.3 H/W ECC and EDC for NAND Flash

Error Correcting Code capable of correcting up to 4 ~ 64 bits in 1Kbytes sector.

6.4 MTBF

MTBF (Mean Time between Failures) of Renice SSD: >4,000,000 hours

6.5 Over voltage and inrush current protection

The over voltage and inrush current protection mechanism of Renice X9 2.5” SATAIII SSD is to deploy a protect circuitry on Device Power In. Once the current or voltage is exceeded, it will be pulled down to the normal value in very short time to protect the drive.

7. Identify Device Parameters

Word	Contents	Description
0	0x004	General information
1	0x3FFF	Number of logical cylinders
2	0x0000	Specific configuration
3	0x0010	Number of logical heads
4 ~5	0x0000	Retired
6	0x003F	Number of logical sectors per logical track
7~8	0x0000	Reserved
9	0x0000	Retired
10~19	0xXXXX	Serial number(20 ASCII characters)
20	0x0003	Retired
21	0x4000	Buffer size. 8MB=0x4000
22	0x0000	Obsolete
23 ~ 26	0xXXXX	Firmware revision(8 ASCII characters)
27~ 46	0xXXXX	Model number
47	0x8010	Number of sectors on multiple commands
48	0x0000	Reserved
49	0x2F00	Capabilities
50	0x4000	Capabilities
51 ~ 52	0x0200	PIO Mode support
53	0x0007	Reserved
54	0x3FFF	Number of current logical cylinders
55	0x0010	Number of current logical heads
56	0x003F	Number of current logical sectors per track
57	0xFC10	Current capacity in sectors
58	0x00FB	Multiple sector setting *. 2,4,8,16 Sectors
59	0x01FF	Multiple sector setting *. 2,4,8,16 Sectors

Word	Contents	Description
60	0x0000	Total number of user addressable sectors(LBA mode only)
61	0x0778	Obsolete
62	0x0000	Obsolete
63	0x0007	Multi-word DMA transfer
64	0x0003	Flow control PIO transfer modes supported
65	0x0078	Minimum Multiword DMA transfer cycle time per word : 120ns
66	0x0078	Manufacturer's recommended Multiword DMA transfer cycle time per word : 120ns
67	0x0078	Minimum PIO transfer cycle time without flow control : 120ns
68	0x0078	Minimum PIO transfer cycle time with IORDY flow control : 120ns
69~74	0x0000	Reserved
75	0x001F	DMA QUEUED command Supports, (32)
76	0x0702	Serial ATA capability
77	0x0000	Reserved
78	0x004C	Support of Serial ATA function
79	0x00xx	Valid of Serial ATA function
80	0x00F8	Major Version Number
81	0x0021	Minor Version Number
82	0x346B	Command set supported
83	0x7F09	Command set supported
84	0x6103	Command set/feature supported extension
85	0x77AB	Command set/feature enabled
86	0xBD23	Command set/feature enabled
87	0x6103	Command set/feature default
88	0x203F	Ultra DMA transfer
89~ 91	0x0003	Reserved
92	0xFFFE	Master Password Revision Code
93	0x0000	Hardware reset result
94~ 99	0x0000	Reserved
100	0x0000	Total number of user addressable sectors in LBA mode

Word	Contents	Description
101	0x0778	-
102	0x0000	-
103	0x0000	-
104~105	0x0000	Reserved
106	0x600x	Physical sector size per sector
107~116	0x0000	Reserved
117~118	0x0100	No of words for logical sectors
119	0x400x	Features Implemented word(supported setting)
120	0x400x	Features Implemented word(Enabled setting)
121-127	0x0000	Reserved
128	0x0001	Security status
129 - 159	0x0000	Undefined
160-205	0x0000	Reserved
206	0x003D	SCT command sets supports
207-209	0x0000	Reserved
210-254	0x0000	Reserved
255	0xxxxx	Check sum

8. ATA Command

Supported ATA8 standard including ATA-ACS2.

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
CHECK POWER MODE	E5h or 98h	Enable Power-Up In Standby	Efh/06h
DEVICE CONFIGURATION	-	Disable Power-Up In Standby	Efh/86h
DEVICE CONFIGURATION FREEZE LOCK	B1h/C1h	Enable DMA Setup FIS Auto-Activate optimization	Efh/10h/02h
DEVICE CONFIGURATION IDENTIFY	B1h/C2h	Disable DMA Setup FIS Auto-Activate optimization	Efh/90h/02h
DEVICE CONFIGURATION RESTORE	B1h/C0h	Enable Device-initiated interface power state transitions	Efh/10h/03h
DEVICE CONFIGURATION SET	B1h/C3h	Disable Device-initiated interface power state transitions	Efh/10h/03h
DOWNLOAD MICROCODE	92h	SET MAX	-
DATA SET MANAGEMENT	06h	SET MAX ADDRESS	F9h/na
EXECUTE DEVICE DIAGNOSTIC	90h	SET MAX FREEZE LOCK	F9h/04h
FLUSH CACHE	E7h	SET MAX LOCK	F9h/02h
FLUSH CACHE EXT	EAh	SET MAX SET PASSWORD	F9h/01h
IDENTIFY DEVICE	ECh	SET MAX UNLOCK	F9h/03h
IDLE	E3h or 97h	SET MAX ADDRESS EXT	37h
IDLE IMMEDIATE	E1h or 95h	SET MULTIPLE MODE	C6h
INITIALIZE DEVICE PARAMETERS	91h	SLEEP	E6h or 99h
NOP	00h/00h	SMART	-
READ BUFFER	E4h	SMART DISABLE OPERATIONS	B0h/D9h
READ DMA	C8h	SMART ENABLE OPERATIONS	B0h/D8h
READ DMA EXT	25h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	B0h/D2h
READ FPDMA QUEUED	60h	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	B0h/DBh
READ LOG EXT	2Fh	SMART EXECUTE OFF-LINE IMMIDIATE	B0h/D4h
READ MULTIPLE	C4h	SMART READ ATTRIBUTE THRESHOLDS	B0h/D1h
READ MULTIPLE EXT	29h	SMART READ DATA	B0h/D0h
READ NATIVE MAX ADDRESS	F8h	SMART READ LOG	B0h/D5h

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
READ NATIVE MAX ADDRESS EXT	27h	SMART RETURN STATUS	B0h/DAh
READ SECTOR(S)	20h	SMART SAVE ATTRIBUTE VALUES	B0h/D3h
READ SECTOR(S) EXT	24h	SMART WRITE LOG	B0h/D6h
READ VERIFY SECTOR(S)	40h	STANDBY	E2h or 96h
READ VERIFY SECTOR(S) EXT	42h	STANDBY IMMEDIATE	E0h or 94h
SECURITY DISABLE PASSWORD	F6h	WRITE BUFFER	E8h
SECURITY ERASE PREPARE	F3h	WRITE DMA	CAh
SECURITY ERASE UNIT	F4h	WRITE DMA EXT	35h
SECURITY FREEZE LOCK	F5h	WRITE FPDMA QUEUED	61h
SECURITY SET PASSWORD	F1h	WRITE LOG EXT	3Fh
SECURITY UNLOCK	F2h	WRITE MULTIPLE	C5h
SEEK	70h	WRITE MULTIPLE EXT	39h
SET FEATURES	-	WRITE SECTOR(S)	30h
Enable write cache	EFh/02h	WRITE SECTOR(S) EXT	34h
Disable write cache	EFh/82h		
Set transfer mode	EFh/03h		

9. SMART

9. 1 SMART sub command sets

In order to select a sub command the host must write the sub command code to the device's Features Register before issuing the SMART Function Set command. The sub commands are listed below.

Command	Command Code(Hex)
SMART READ DATA	D0h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
SMART READ LOG	D5h
SMART WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh
SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	DBh

9. 2 SMART Read Data (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. The Attribute Values consist of 512bytes.

9.2.1. Device Attribute Data Structure

Byte	Description
0~1	Data structure revision number (Vendor Specific)
2~361	1st - 30th Individual attribute data (Vendor Specific)
362	Off-line data collection status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability

368~369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point (Vendor Specific)
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374~510	Reserved
511	Data structure checksum

9.2.2. Individual Attribute Data Structure

COMMAND CODE B0h with a Feature Register value of D9h
PROTOCOL Non-data. INPUTS

0	Attribute ID Number
1~2	Flags
3~10	Attribute Value(FFFF FFFF FFFF FFFFh)
11	Reserved

9.2.3. Attribute ID Numbers

ID	Attribute Name	ID	Attribute Name
0	(Indicates unused attribute data)	199	Total count of write sectors
1	Raw Read Error Rate *	200	Total count of error bits from Flash
9	Power-On Hours	201	Total count of read sectors with correctable bit errors
12	Power On Count	202	bad block full flag
184	Init Bad Block Count	203	Max PE Count Spec.
195	Program Failure Block Count	204	Erase Count Min
196	Erase Failure Block Count	205	Erase Count Max
197	Read Failure Block Count (uncorrectable bit errors)	206	Erase Count Average
198	Total count of read sectors	207	Remaining Life[%]

* indicates that the corresponding Attribute Values is fixed value for compatibility.

9.3 SMART Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature.

9.4 SMART Save Attribute Values (subcommand D3h)

This subcommand causes the device to start the off-line process for the requested mode and operation.

The LBA Low register shall be set to specify the operation to be executed.

LBA Low	Description
00h	Execute SMART off-line data collection routine immediately
01h	Execute SMART Short self-test routine immediately in off-line mode
02h	Execute SMART Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute SMART Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute SMART short self-test routine immediately in captive mode
82h	Execute SMART Extended self-test routine immediately in captive mode
84h	Execute SMART selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (see Table 7-1: －Device Attribute Data Structure‖ on page 23) and ATA registers and then executes the command completion. See definitions below.

Status Set ERR to one when the self-test has failed

Error Set ABRT to one when the self-test has failed

LBA Low Set to F4h when the self-test has failed

LBA High Set to 2Ch when the self-test has failed

9.5 SMART Read Log Sector (subcommand D5h)

This command returns the specified log sector content to the host.

LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

Log Sector Address	No. Sector	Content	
00h	1	Log directory	Read Only
01h	1	SMART error log	Read Only
02h	1	Comprehensive SMART error log	Read Only
04h-05h	-	Reserved	Read Only
06h	1	SMART self-test log	Read Only
08h	-	Reserved	Read Only
09h	1	Selective self-test log	Read and Write
0Ah-7Fh	-	Reserved	Read Only
80h-9Fh	16	Host vendor specific	Read and Write
A0h-FFh	-	Reserved	Vendor Specific

9.5.1 Self-test log structure

Byte	Description
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life time stamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
……	……
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

N is 0 through 20.
The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

9.5.2 Self-test log structure

Byte	Content	
0-1	Data structure revision	Read and Write
2-9	Starting LBA for test span 1	Read and Write
10-17	Ending LBA for test span 1	Read and Write
18-25	Starting LBA for test span 2	Read and Write
26-33	Ending LBA for test span 2	Read and Write
34-41	Starting LBA for test span 3	Read and Write
42-49	Ending LBA for test span 3	Read and Write
50-57	Starting LBA for test span 4	Read and Write
58-65	Ending LBA for test span 4+	Read and Write
66-73	Starting LBA for test span 5	Read and Write
74-81	Ending LBA for test span 5	Read and Write
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags R/W	Read and Write
504-507	Vendor Specific	Vendor Specific
508-509	Selective self test pending time	Read and Write
510	Reserved	Reserved
511	Data structure checksum	Read and Write

9.6 SMART Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector.
LBA Low and Sector Count registers shall be set to specify the log address and sector number to be written.

9.7 SMART Enable Operations (subcommand D8h)

This subcommand enables access to all SMART capabilities. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

9.8 SMART Disable Operations (subcommand D9h)

This subcommand disables all SMART capabilities. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.
After receipt of the SMART Disable Operations subcommand from the host, all other SMART subcommands except SMART Enable Operations are disabled and will be aborted by the device returning the error code as specified in :SMART Error Codes.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or a SMART Save Attribute Values command.

9.9 SMART Read Log Sector (subcommand D5h)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

9.10 SMART Read Log Sector (subcommand D5h)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities. The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count Feature Description

00h Disable Automatic Off-line
F8h Enable Automatic Off-line

10. Ordering Information

Capacities/Flash type	Standard Temp.	Industrial Temp.
8GB/SLC	RCS008-SX92	RIS008- SX92
16GB/SLC	RCS016- SX92	RIS016- SX92
32GB/SLC	RCS032- SX92	RIS032- SX92
64GB/SLC	RCS064- SX92	RIS064- SX92
128GB/SLC	RCS128- SX92	RIS128- SX92
256GB/SLC	RCS256- SX92	RIS256- SX92
512GB/SLC	RCS512- SX92	RIS512- SX92
640GB/SLC	RCS640- SX92	RIS640- SX92
8GB/MLC	RCM008-SX92	RIM008- SX92
16GB/MLC	RCM016- SX92	RIM016- SX92
32GB/MLC	RCM032- SX92	RIM032- SX92
64GB/MLC	RCM064- SX92	RIM064- SX92
128GB/MLC	RCM128- SX92	RIM128- SX92
256GB/MLC	RCM256- SX92	RIM256- SX92
512GB/MLC	RCM512- SX92	RIM512- SX92
640GB/MLC	RCM640- SX92	RIM640- SX92

11. Product Part Number Naming Rule